Docket No. 0756-1838

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	Art Unit: 2822
Shunpei YAMAZAKI et al.	)	Examiner: M. Guerrero
Serial No. 09/118,010	)	
Filed: July 17, 1998	)	
For: SEMICONDUCTOR DEVICE, METHOD OF FABRICATING SAME, AND ELECTROOPTICAL DEVICE	)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with The United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on 9/4/02

RESPONSE

Honorable Commissioner of Patents
Washington, D.C. 20231

Sir:

The Official Action mailed June 4, 2002 has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time.

Applicants note with appreciation the consideration of the Information Disclosure Statements filed on July 17, 1998; March 21, 2000; April 25, 2000; July 17, 2000; November 30, 2000; March 9, 2001; April 11, 2001 and November 2, 2001.

Claims 1-8 and 11-73 are pending in the present application, of which claims 11-12, 18, 23, 28, 33, 38, 40, 43, 47, 53, 59, 64 and 69 are independent. Applicants note with appreciation the allowance of claims 1-8 and 11-46. For the reasons set forth in detail below, all claims are believed to be in condition for allowance and favorable reconsideration is requested.

Paragraph 2 of the Official Action rejects claims 47-73 as obvious based on the combination of U.S. Patent 5,055,899 to Wakai et al. and U.S. Patent 5,427,961 to Takenouchi et al. As stated in MPEP § 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the

prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Applicants note that all of the rejected claims 47-73 recite an interlayer insulating layer comprising a resinous material provided over a thin film transistor in the same way as allowed claims 1-8 and 11-46. As previously noted in the Amendment filed July 17, 2000, a resinous substrate has poor heat resistance (see page 2, lines 25-29 of the specification). Accordingly, it is preferable when using a resinous substrate to use a lower temperature process during forming a thin film transistor (TFT) on such a substrate. In case of forming the interlayer insulating layer comprising silicon oxide or silicon nitride over the resinous substrate by plasma CVD (PCVD), the resinous substrate is often damaged because the substrate is generally heated at a temperature of 300° C or more.

On the other hand, in accordance with the present invention, a resinous interlayer insulating layer can be formed by a coating method at a lower temperature than with PCVD without damaging the resinous substrate. Thus, the resinous interlayer insulating layer is preferable for use with the resinous substrate in view of the TFT forming process. Neither Wakai nor Takenouchi disclose or suggest these advantages achieved by the present invention.

Furthermore, the resinous interlayer insulating layer has an advantage of providing the top surface of the TFT with a planarized surface, in a similar manner in which the resinous layer over the resinous substrate provides the bottom surface of the TFT with a planarized surface. In addition, where a device is subject to bending, the

use of a resinous interlayer insulating layer and the resinous layer on the resinous substrate is advantageous to reduce undesirable effects to the TFT caused by bending due to their higher flexibility compared to that of other insulating materials.

Thus, since the advantages of using a resinous substrate with a resinous layer and a resinous interlayer insulating layer for reducing harmful effects of bending on the TFT are neither disclosed or suggested by Wakai or Takenouchi, whether taken alone or in combination, it is respectfully submitted that a *prima facie* case of obviousness cannot be maintained and favorable reconsideration is requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789